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by

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Lieutenant, United States Navy

Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

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ABSTRACT

The increased use of digital data handling systems and the consideration of pulse code modulated telemetering systems have given rise to a widespread interest in the problem of analog-to-digital conversion. This paper defines the basic design problems presented by a transistorized, ten-bit, high speed (100 kc.) converter. Moreover, a feasible converter which will meet these specifications is described herein. The paper describes a direct voltage weighting technique which provides greater system accuracy than that offered by a current summing network, under normal processes of production. Results of the comparison between weighting methods lead to further conclusions concerning the accuracy limits capable of being realized in such converters at the present time.

The author wishes to express his appreciation to Professors M. L. Cotton and W. M. Bauer of the U. S. Naval Postgraduate School and to Mr. W. P. Klemens of the Pacific Division, Bendix Aviation Corporation for their assistance and encouragement in the accomplishment of this work.

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LIST OF ILLUSTRATIONS

LIST OF SYMBOLS AND ABBREVIATIONS

Symbol	Meaning
ADCON	Analog-to-digital converter.
DACON	Digital-to-analog converter.
T_i	Denotes the ith toggle in the binary register, where i signifies the order of the toggle; for example, T_0 contains the least significant bit or 2^0, and T_9 contains 2^9.
A_i	Denotes the SET input for T_i; that input which when subjected to a positive trigger will put the toggle in the positive or "1" state.
B_i	Denotes the RESET input for T_i; a positive trigger applied to this input will place the toggle in the lower state, "0".
D_j	Denotes the jth digit time in the logic network; a digit time being the time required for a single comparison step during conversion.
Z	Output of the voltage comparator; this output occurs when the analog input voltage is less than the feedback analog voltage from the DACON.

1. INTRODUCTION.

An increased consideration of digital techniques in such fields as data handling and processing, switching, automation, data transmission, and computing has produced a definite need for the development of analog-to-digital converters. The majority of data measuring components (transducers) of the present time produce an electrical signal which is an analog representation of the data being measured. In order for such data to be used subsequently in digital systems, these forms of information must be converted accurately into digitalized form.

What has created this interest in digital techniques? In a data handling process, the accuracy of the data and the maintenance of that accuracy throughout the span of the process are of paramount importance to the user. In a lengthy system, an analog signal may suffer considerable degradation as it passes through successive stages of the system, leading to unacceptable errors and/or complex calibration processes. Digital data, in the form of a pulse code for example, may be processed repeatedly with little or no loss in accuracy. The digital system is faced with the problem of recognizing merely the presence or absence of a pulse in a specific location within a pulse train. This fact means, further, that a pulse coded signal is more easily detected under conditions of reduced signal to noise ratio. These advantages do not mean that a pulse code system is a panacea for all ills experienced in analog systems, nor do they mean

that there are no disadvantages to the digital system. A pulse code system is inherently more complex than its analog counterpart. For example, in a multi-channel telemetering application, the accuracy determining components of a PCM and an FM/FM system are the analog-to-digital converter and the sub-carrier oscillators, respectively. In the former all channels of information are passed through a single unit; thus, the failure of this single ADCON would mean complete failure of the system. On the other hand, the failure of a single sub-carrier oscillator would produce failure in one or, at most, two channels. In like manner, errors produced in each of these components would result in complete or partial system inaccuracy, respectively. The examples cited show that digital techniques offer promise in certain fields, yet do not imply the abolition of analog systems in all applications.

The analog-to-digital converter is the key component in systems whose normal input is an analog signal. The accuracy of the data in the system is established, essentially, by the ADCON and the stages which precede it. Succeeding stages must recognize only a "pulse, no pulse" condition. Thus, it is appropriate that a glance be taken at the fundamentals of converter design and the present state of the art.

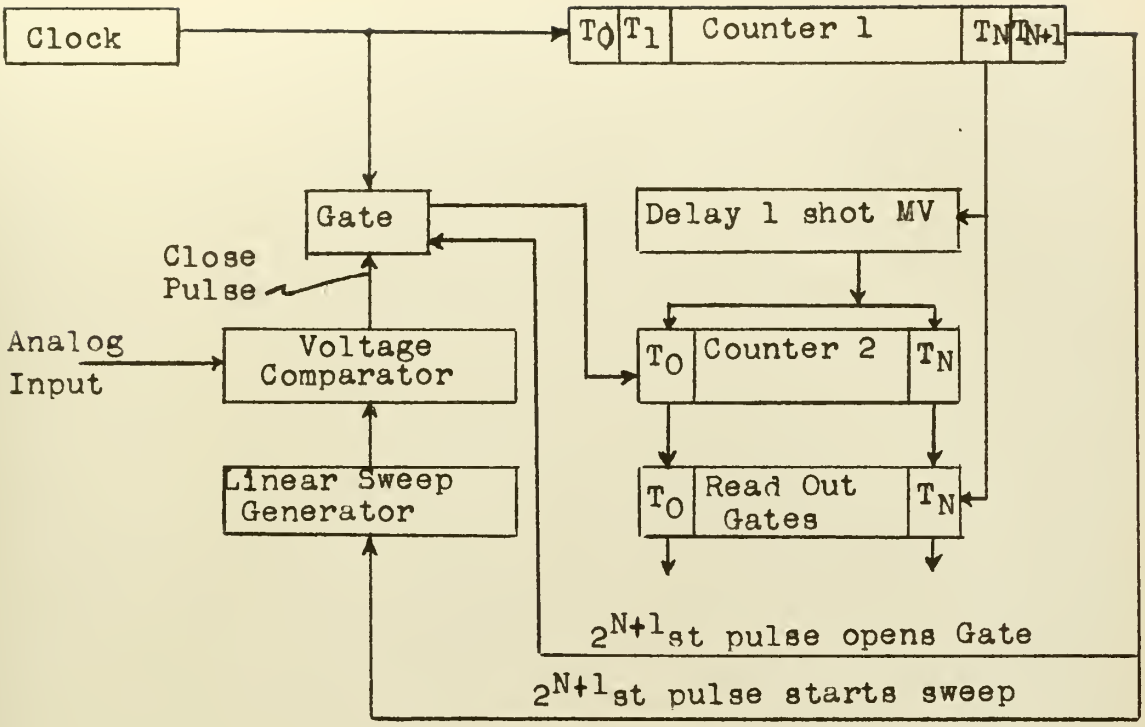
Although there are electromechanical methods of conversion, the investigation has been restricted to those techniques which are "all electronic" for obvious reasons. There are three fundamental methods for accomplishing analog-to-

digital conversion:[1]

1. Time encoding (essentially a time measurement); also called time-base or sweep-time encoding.
2. Feedback encoding (essentially a voltage comparison); also called voltage-comparison encoding or encoding by parts.
3. Space encoding (essentially a physical representation of the code).

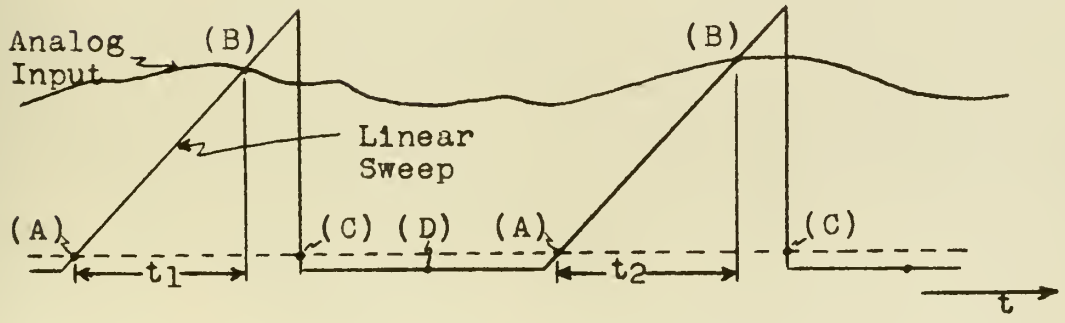
A typical time encoding system is shown in Figure 1. The two major problems presented by such a system lie in ensuring the linearity of the sweep and in the speed limitations imposed by the necessity to count serially. The upper limit in speed of conversion for a ten-bit system is about 10,000 conversions per second, based on a flip flop capable of ten megacycle operation in a counter. The accuracy of the system is determined, primarily, by the sweep's linearity. Advantages offered by this method are circuit simplicity, construction ease, and the absence of extensive logic circuits. Figure 2 displays the principle of time-base encoding. The block diagram of Figure 1 shows an N-bit system. Counter 1 is an N + 1-bit binary counter which is triggered continuously by pulses from the clock. In this example, an extra bit has been added to the counter in order to allow one-half of each conversion cycle for recovery of the sweep generator, read out, and stabilization of all circuits prior to the next sample. The 2^{N+1}st pulse opens the gate and starts the sweep. The open gate then allows clock pulses to trigger

[1]M. L. Klein, F. K. Williams, and H. C. Morgan, "Analog-to-Digital Conversion", Instruments and Automation, Vol. 29, pg. 911, May 1956.



Typical Time Encoding System

Figure 1

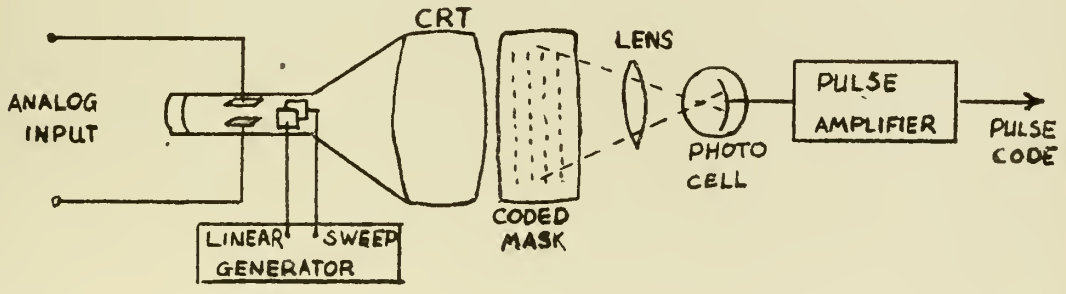


Principles of time encoding

Figure 2

Counter 2, which is the timing counter. Its count continues from point (A) to coincidence at point (B) which occurs when the voltage comparator senses an equality between the analog input and the sweep amplitude. The gate is closed upon signal from the comparator, thereby stopping the count of Counter 2. Thus, it can be seen from Figure 2 that the time t_1 measured in the counter is a direct representation of the sweep amplitude at coincidence, if the sweep is linear. The time is in the form of a binary number which can be "read out" into a digital system. The 2^Nth pulse from Counter 1 triggers the delay multivibrator and the read out register simultaneously; point (C). The delay multivibrator waits about one-fourth the conversion cycle, then resets all the toggles in the timing counter, point (D), ensuring that the read out has been completed and that all components will have time in which to "prepare" for the next conversion.

A typical spatial encoding system is shown in Figure 3. This example employs a cathode ray tube which scans a binary coded raster to produce the binary digit. This system is

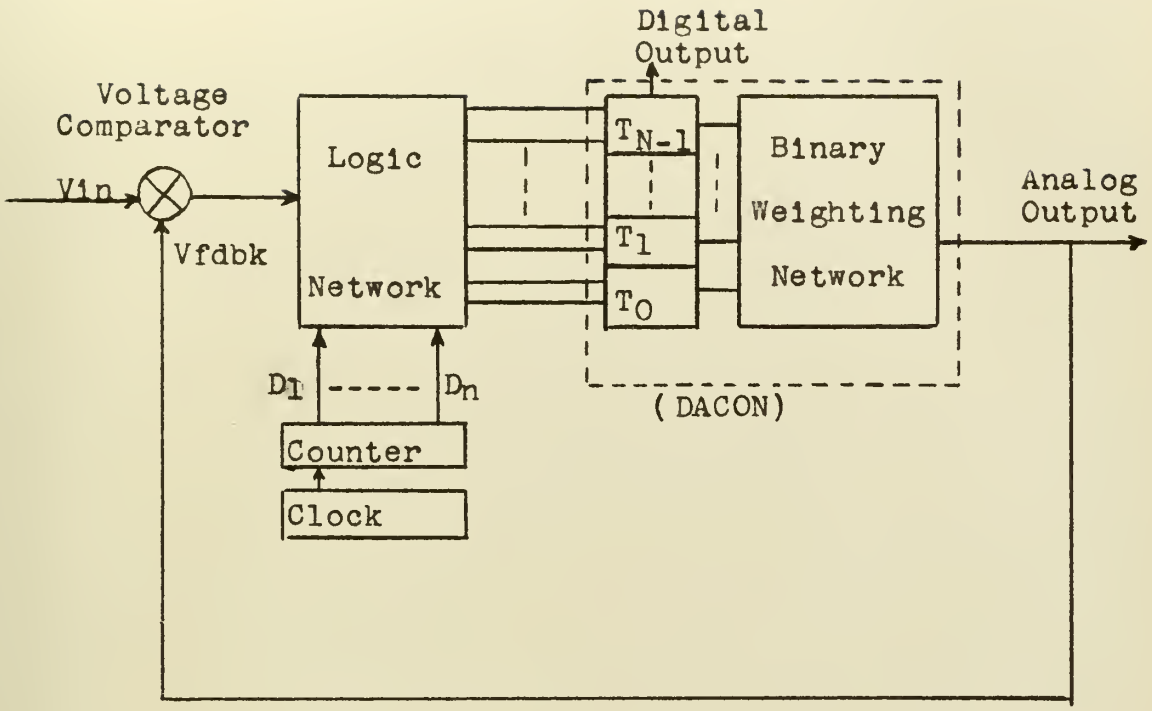


Typical CRT Spatial Encoding System

Figure 3

the most direct of the three fundamental techniques discussed. As in the time encoding system, there are virtually no logic circuits or matrices needed. By virtue of its inate simplicity it is the fastest method presently available. Using a monoscope tube, it is possible to achieve conversions speeds up to ten megacycles with a ten-bit system. In the system shown, the analog input is applied to the vertical deflection plates, thus positioning the electron beam vertically in proportion to the input amplitude. The linear sweep generator is applied to the horizontal deflection plates to sweep the electron beam across the binary code at the level determined by the analog input. The code thus scanned is focussed at the photo cell which passes it to the pulse amplifier. It is obvious that ambiguities could arise if the electron beam were positioned vertically on a division between two codes. This example would be restricted in speed by the relatively slow response of the photo cell. Moreover, such a system would be used normally with relatively high level inputs.

A functional block diagram of a basic feedback encoder is shown in Figure 4. Although it is the least developed of the techniques, it appears to hold considerable promise. Perhaps one reason for its lag in development lies in the fact that it involves more complex circuitry by nature. The increased complexity results from the extensive logic and switching circuits required of the method. The current speed capabilities of this method extend to about 200,000 samples



Basic Feedback Encoding System

Figure 4

per second. A system of this type employs a digital-to-analog converter (DACON) to produce a feedback analog signal which can be compared with the unknown analog input. If the comparison were accomplished in single digit steps until equality occurred between the two signals, the operation would be that of a time encoder. By the use of an iterative scheme of successive approximations, the comparison may be accomplished in a number of steps equal to N, the number of bits in the system. Thus, the speed of conversion can be improved by an order of magnitude. N comparisons will always produce a number in the binary register which is within the least significant bit of the input amplitude. The weighting network is designed such that when the register is filled, (i. e., 1111111111) the feedback analog is at the maximum value of expected input swing. The first comparison is made with the register set to 1000000000, or one-half full scale. If the input is greater than the feedback signal, the toggle containing the most significant bit (T_9) remains "set". If the input is less than the feedback signal, this toggle must be "reset". The next toggle (T_8) is always "set", to produce either 1100000000 or 0100000000, dependent upon the state of T_9 as determined by the previous comparison. This process continues through each of the toggles in the register until all the bits have been sampled, N steps. The register then contains a binary number which is within $1/2^N$ of the input signal. The logic consists of a clock whose frequency is 1/N times the conversion frequency, a counter to produce the

digit times, and the decision circuits necessary to control the state of the toggles in the register. Since the next toggle in line is always "set" at the commencement of each comparison step, and since action on the preceding toggle need be taken only when the input is less than the feedback signal, the logic circuitry will be standard, fast logic.

Table I lists some analog-to-digital converters which are available at the present time:

TABLE I

Name	Manufacturer	Characteristics
DATRAC	Epsco, Inc.	10-bit; 50 kc. [14]
ADAR	Radiation, Inc.	8-bit; 24 kc. [9]
IDIOT II	Rocketdyne Div., North American Aviation Corp.	10-bit; 100 kc. [14]
Rea-converter	J. B. Rea Co.	12-bit; 100 kc. [14]
Experimental	Herring, Lamb	10-bit; 100 kc. [4]
- - - -	Hoover Electronics	11-bit; 45 kc. [5,6]
- - - -	Ramo-Wooldridge Corp.	9-bit; 8.3 kc. [11]
- - - -	Packard-Bell	14-bit; 50 kc.

These ADCONs represent a large portion of the spectrum of present day converters which employ the feedback method. The Rea-converter is a large device employing vacuum tubes and possessing high power requirements. The Ramo-Wooldridge unit, on the other hand, is a small transistorized unit which requires about 20 watts of power.

2. ANALOG-TO-DIGITAL CONVERTER DESIGN CONSIDERATIONS.

The objective of this investigation is to study the design features of a low power, high speed analog-to-digital converter for possible applications in PCM telemetering systems and in receivers which employ correlation techniques. The specifications for such a converter are:

Resolution	10-bits (.1%).
Conversion speed	100 kc.
Input level	0-5 volts.
Power	15-20 watts.

The feedback encoding method has been chosen for the converter, as it is the only means by which all of the listed specifications can be achieved in a single unit. The time-base technique can be disqualified immediately due to its limitations in speed. The inherent simplicity of a cathode ray tube spatial system may be lost due to a need for special codes to avoid ambiguity when the electron beam is positioned on the border of two separate levels. The cathode ray tube implies a high level system, displays poor stability under severe environmental conditions such as might be expected in a missile telemeter, and requires more power than that listed in the specifications. A feedback system employing semiconductors promises to fulfill all the specifications and, ultimately, the stability criteria of a missile application. The converters listed in Table I of the preceding section possess all of the specifications collectively, but no single unit can claim all of them. Thus, the ADCON under study can

fill a gap existing in the present spectrum of converters, if the unit is feasible.

There are two major problems confronting the designer of such a converter at first glance. The first is that of designing an accurate weighting network which will produce binary increments of analog information while being switched at speeds of about one megacycle. This problem divides itself, further, into a search for an optimum network of weighted resistors and a search for fast, accurate switches. The second major problem is one of finding a transistorized voltage comparator, which will be sensitive to a difference input of five millivolts and will produce an output capable of performing logic in the succeeding stage under such an input condition. The logic circuitry will be fast, standard logic requiring no advance in the state of the art. The bistable multivibrator to be used in the binary register and in the counter must be capable of high speed operation, but the switching speed required is well below the upper limit of present semiconductors. The investigation is divided into five broad phases:

a. Design of a basic bistable multivibrator to operate at speeds up to two megacycles.

b. Investigation and design of a binary weighting network and its associated switches, which, in combination with a ten-bit register, will constitute the digital-to-analog conversion unit of the system.

c. Design of a voltage comparator sensitive to five millivolts input.

d. Design of the logic network.

e. Marriage of these components into a complete "pilot" system.

This paper is devoted almost exclusively to phases a and b, which have been completed successfully. Minor design refinements to an existing voltage comparator will complete phase c, and the testing of the straight-forward logic network will complete phase d. The final phase will entail extensive tests of the system, during which time the problems of packaging and environmental stability must be considered in the light of the individual's specific task for the unit. The variables in the final phase are of such an individual nature that this paper has been confined to the study of the first four phases only.

3. BASIC BISTABLE MULTIVIBRATOR

A bistable multivibrator is required for use in the binary register and in the counter of the logic network. There are ten comparison steps to be made during each conversion cycle and, possibly, two additional steps to allow for a synchronizing signal and a "read out" command. With allowances for variations in the logic requirements, each flip flop should be capable of switching at speeds up to two megacycles.

There are two considerations to be made in selecting the appropriate transistor for the multivibrator:

a. The transistor must possess a frequency response which is considerably greater than the switching speed desired of the circuit.

b. The transistor must be capable of producing a relatively large output swing, which can conceivably control the switches in the weighting network.

Silicon switching transistors capable of speeds as high as 300 megacycles are presently available. An example is the 2N501 which is produced by the Lansdale Division of Philco. This device achieves its high speed through the fact that low level supply voltages are used, thereby limiting the output swing to less than three volts. This class of transistor is relatively expensive even in large lot purchases. A Germanium transistor, the RCA 2N247 Drift Transistor possesses a high alpha cut-off frequency, and although not designed for specific use in switching applications, it has

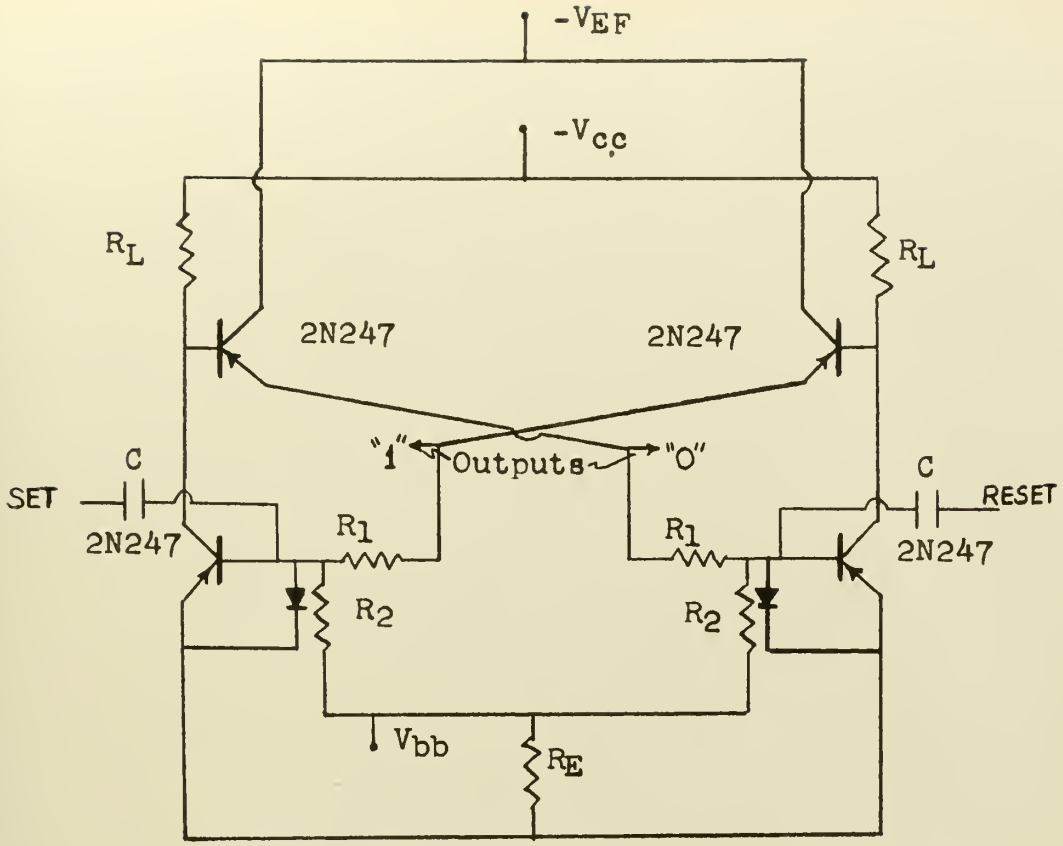
been used in some multivibrator designs. It has the advantage that it is normally used with larger voltage supplies than the Silicon switching transistors and is capable of producing correspondingly larger output swings. Its cost is approximately one-sixth that of the typical high speed Silicon switching transistor. On the basis of these facts, the 2N247 was chosen for the initial design.

The steps leading to the final design, which is shown in Figure 5, are described in Appendix A. The final circuit is a non-saturating, set-reset bistable multivibrator which employs two additional transistors as emitter followers in the collector circuits of the switching transistors. These emitter followers accomplish two functions:

a. Improve the shape of the output pulse.

b. Act as buffers against loading by succeeding stages.

The diodes placed between the base and emitter of each of the switching elements prevent exceeding the maximum dc voltage rating from base-emitter (1 volt). The emitter followers have been collector-biased in such a manner that they will always be in the high frequency response region of their characteristics. As the collector bias drops below a value of about three volts, the alpha cut-off frequency also falls markedly. A sketch of the waveform produced by the toggle is shown in Figure 5. A 1.5 volt trigger is sufficient to change the state of the flip flop, when applied to the base of the switching transistor. Distortion begins when the trigger exceeds 6 volts. The circuit is independent of



Final component values:

V_{EF} = -8 volts

V_{cc} = -2 volts

V_{bb} = 29 volts

R_L = 3.3K

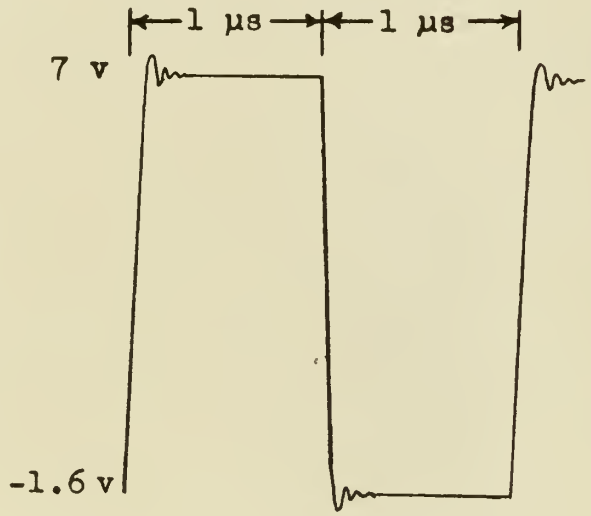
R_1 = 6.8K

R_2 = 1.0K

R_E = 1.3K

C = 15 μμf

Diodes are 1N625.



Bistable multivibrator

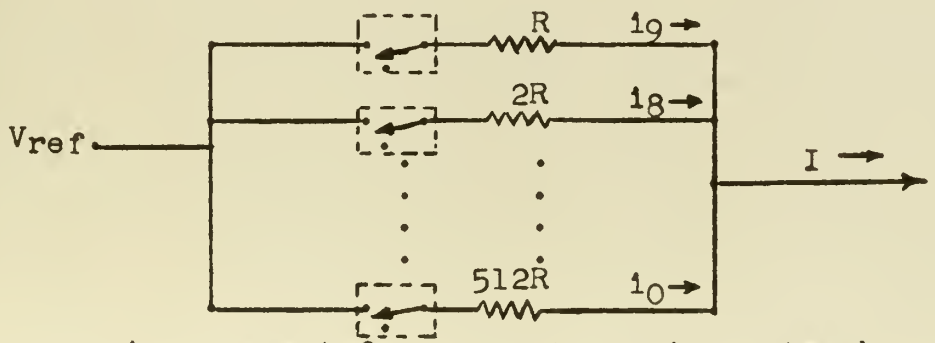
Figure 5

transistor "Beta" by design; so no selection process is necessary in the production of the multivibrator. The pulse at the output has been observed at switching frequencies ranging from one megacycle to one kilocycles with no change observed in output waveforms. When left in a given state overnight, output levels showed no noticeable deviation. Each flip flop requires 334 milliwatts of power. This fact means that the ten-bit register will require 3.34 watts.

4. BINARY WEIGHTING NETWORK PRINCIPLES

The binary weighting network is a collection of resistors whose function it is to produce an analog representation of the binary number which is stored in the register at that moment. Its output will be in the form of either a weighted voltage or current. In a ten-bit system the network must be capable of providing 1024 discrete levels of analog information to correspond to the numbers possible in the register. The use of a binary numbering system suggests the possibility of using ten weighted resistors, each of which can be in one of two available states as controlled by a specific toggle.

Such a network is realizable by summing incremental currents at a single node. These increments may be produced either by supplying weighted reference voltages to ten parallel branches containing resistors of equal value, or by supplying a single reference voltage to ten parallel paths containing weighted resistors. The latter case is shown in Figure 6. This arrangement would produce increments of



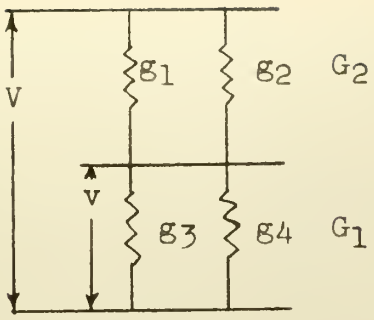
Arrangement for current summing network.

Figure 6

current which were binary weighted in those branches which were switched to the voltage supply. I equals the sum of all branch currents flowing into the summing node at a given time. It is obvious that increments of current equal to 1/2, 1/4, to 1/1024 will be produced in paths 9, 8, to 0, respectively. The fractions are with respect to unity; that is, when all increments of current are flowing into the summing node. The two current summing techniques are widely used in present ADCONs. Packard-Bell refers to its weighting network as a "Voltage Divider", but the actual operation of the network is not available, apparently for proprietary reasons.

The fact that the current summing technique is employed so widely and that no voltage weighting technique is discussed as such in the literature led to an initial consideration of a voltage network. A voltage divider consisting of resistors in series is out of the question, since it would need 1024 elements and an excessive number of switches in the ten-bit system. If this were the only way of realizing such a network, the current summing method could accomplish the same objective much more economically and practically. An article[18] suggesting an arrangement for switching resistors in a manner to produce a decimally weighted voltage output led to the voltage divider arrangement shown in Figure 7. Herein lies a realizable voltage weighting network which uses ten resistors and ten switches, and which possesses attributes similar to those of the current network described

(a)

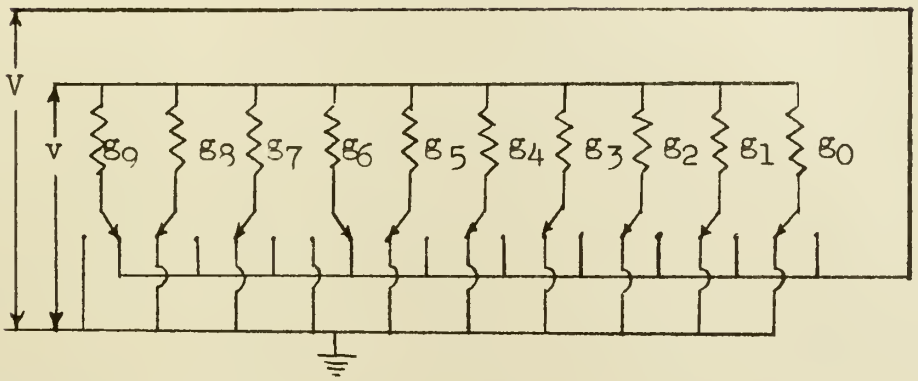


$G_1 = g_3+g_4$; $G_2 = g_1+g_2$.

$V = I(\frac{G_1-G_2}{G_1G_2})$; $v = I/G_1$.

$v = V(\frac{G_2}{G_1+G_2})$

(b)



Relative values:

g_0	1	r_0	512
g_1	2	r_1	256
g_2	4	r_2	128
g_3	8	r_3	64
g_4	16	r_4	32
g_5	32	r_5	16
g_6	64	r_6	8
g_7	128	r_7	4
g_8	256	r_8	2
g_9	512	r_9	1

Ex: in (b), g_9 & g_6 are in G_2.

Binary number = 1001000000 =

$2^9+2^6 = 512+64 = 576$.

$G_2 = g_9+g_6 = 512+64 = 576$

$G_1+ G_2 = 1023$

$v = V(\frac{576}{1023})$

Voltage divider network

Figure 7

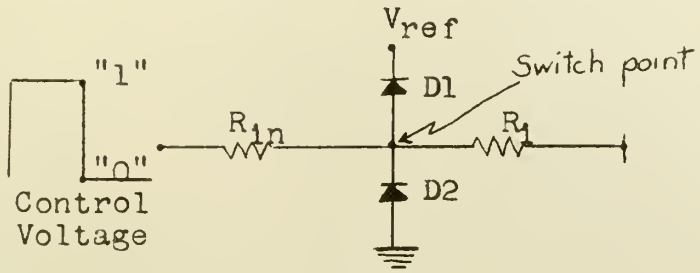
earlier. A comparison of the two techniques is made in Section 6 of this paper. In calculations for the network of Figure 7, relative values of conductance have been used because of their values are additive for parallel combinations such as this. The resistors (conductances) are switched between ground and a reference voltage equal to 1023/1024 of the full value which the system will accept. By controlling each switch with the appropriate toggle, a directly weighted voltage output can be produced. The reason for the apparent discrepancy of the reference voltage lies in the fact that the ten-bit register, when filled, can never exceed the decimal equivalent of 1023.

5. DIODE SWITCHES.

The functional diagram of the divider arrangement which was shown in Figure 7(b) depicts ten switches, each of whose action is that of a double-throw, double-pole switch. The position of each switch is dependent upon the state of the specific toggle with which the resistor is associated. It is the switch which enables each resistor to be placed in either G_1 or G_2 of the parallel arrangement of elements. Essentially, the switch consists of two transmission gates; on one side the reference voltage must be passed with minimum loss to the switch point of the element, and on the other side a dc ground potential must be passed to that same switch point. The action of the two gates as a single switch must be such that when one gate is open, the other gate must be closed, thereby isolating the switch point from the undesired potential. The most desirable method of controlling the action of the switch is with a single source; i. e., one of the outputs of the preceding toggle.

Diode gates are desirable in this application because of their unilateral and passive characteristics. If the "perfect diode" were a reality, a two-diode switch such as that shown in Figure 8 would be ideal. With the control voltage at its high level, D1 would be forward-biased and D2 would be back-biased, presenting a shorted path from the reference voltage to the switch point and an open circuit between the switch point and ground, respectively. With the control voltage in the opposite state the diode biases would

be reversed. However, the perfect diode does not exist in fact, and the .3 to .5 volt drop which exists across the forward-biased diode introduces an unacceptable error in a low level system such as the five volt unit under design.



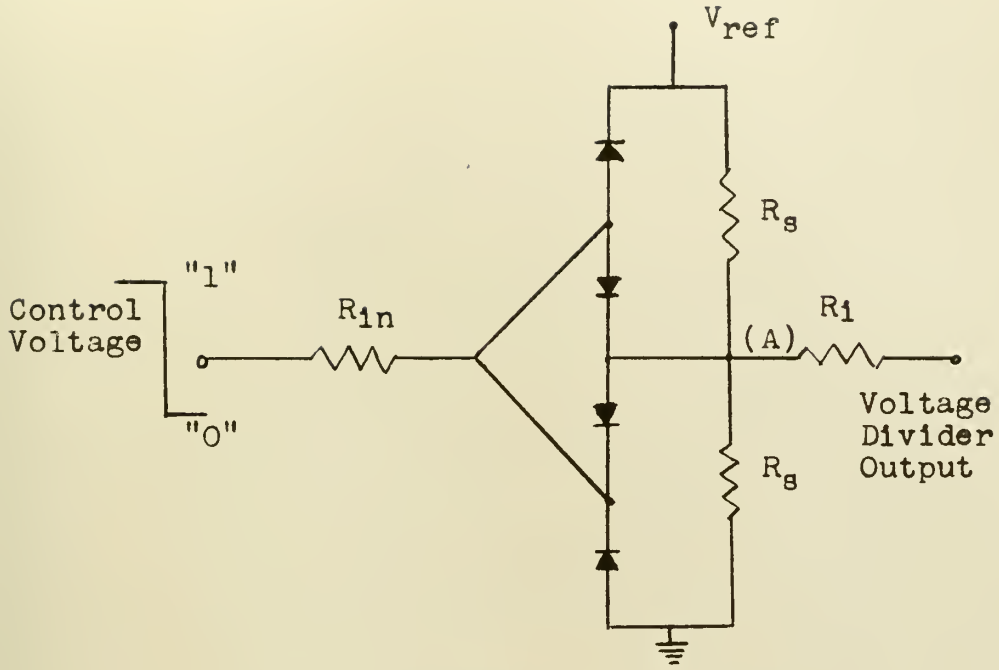
Ideal two-diode switch using "perfect diodes".

Figure 8

In consideration of the transmission gate design, it is found that two criteria must be met; first, the voltages must be passed without errors being introduced by the gate itself, and second, the gate must be capable of feat in an interval time which is dictated by the specified conversion speed of the system. These criteria cannot be treated independently, as the improvement of one tends to degrade the other. [1, 10, 16, 19] Basically, the accuracy of the gate can be improved by increasing the number of diodes employed in the gate. This improvement is accomplished by the fact that multiple paths are provided by the additional diodes, and that two forward-biased diodes tend to compensate for each other's forward voltage drop. This concept is enhanced by the realization that the diodes display a fairly constant forward drop over a range of current values. Fundamentally, the increase in diodes tends to degrade the speed in which the gate will accomplish its switching action. The

recovery time of a diode switch is based upon the RC time constant which is a function of the capacitance introduced into the circuit by the diode and of the equivalent resistance of the circuit. Thus, the addition of parallel diode branches increases the total capacitance of the circuit with no accompanying reduction in the equivalent resistance of the circuit. In the final switch, the realization of both accuracy and speed becomes a compromise.

Two circuits which will perform the desired switching functions are shown in Figures 9 and 10. The first is a functional four-diode switch which consists of two two-diode transmission gates. There is some compensation for the forward drops with the use of the additional diodes, but it is extremely conditional upon the matching of diodes and the value of R_s. The resistor, R_s, serves the twofold function of compensation and of furnishing a continuous path to ground for the reference voltage supply. Although the switch is capable of performing the task, its accuracy is critical of the control voltage levels. With R_s fixed slight changes in the control voltage produce excessive errors in the weighted voltage output. This discrepancy can be corrected by designing the toggle in such a manner that its stability will permit the use of this switch, but it is more desirable to use a switch which possesses the stability over a range of control voltage variations. Moreover, the control voltage required by this switch is of a large swing. With the toggle design described for the system, an amplifier would be required



Circuit values:

R_{in} = 900 ohms

R_s = 1K

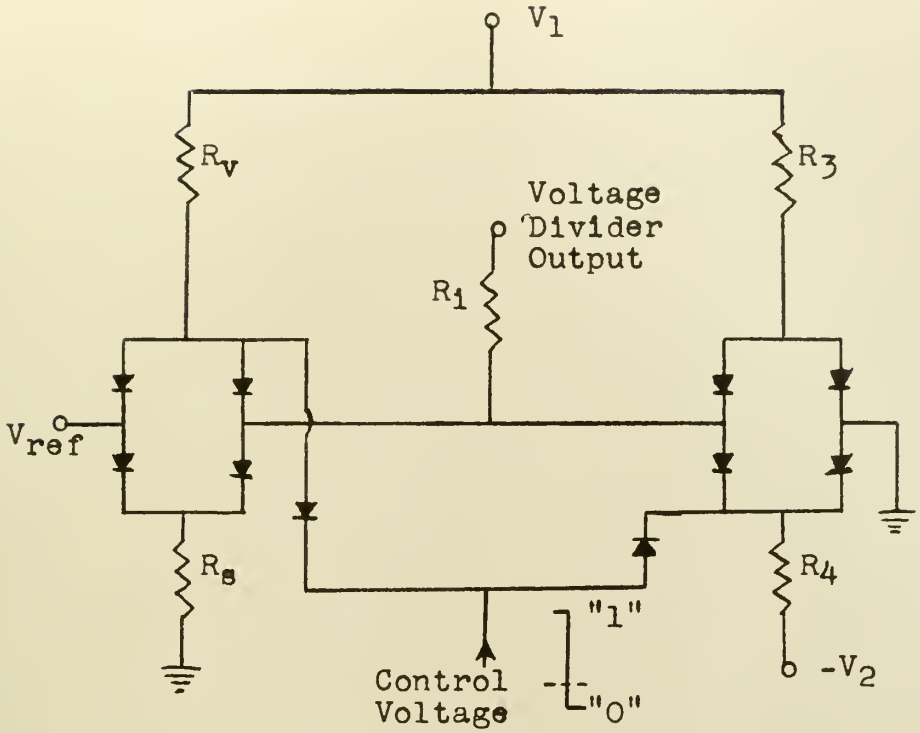
R_i = ith weighting resistor

V_{ref} = 4.995 volts

Diodes: 1N625

Four-diode switch

Figure 9



Circuit values:

V_1 = 13 volts

$-V_2$ = -10 volts

V_{ref} = 4.995 volts

R_v = 2.2K

R_s = 1.5K

R_3 = R_4 = 4.3K

R_i = ith weighting resistor

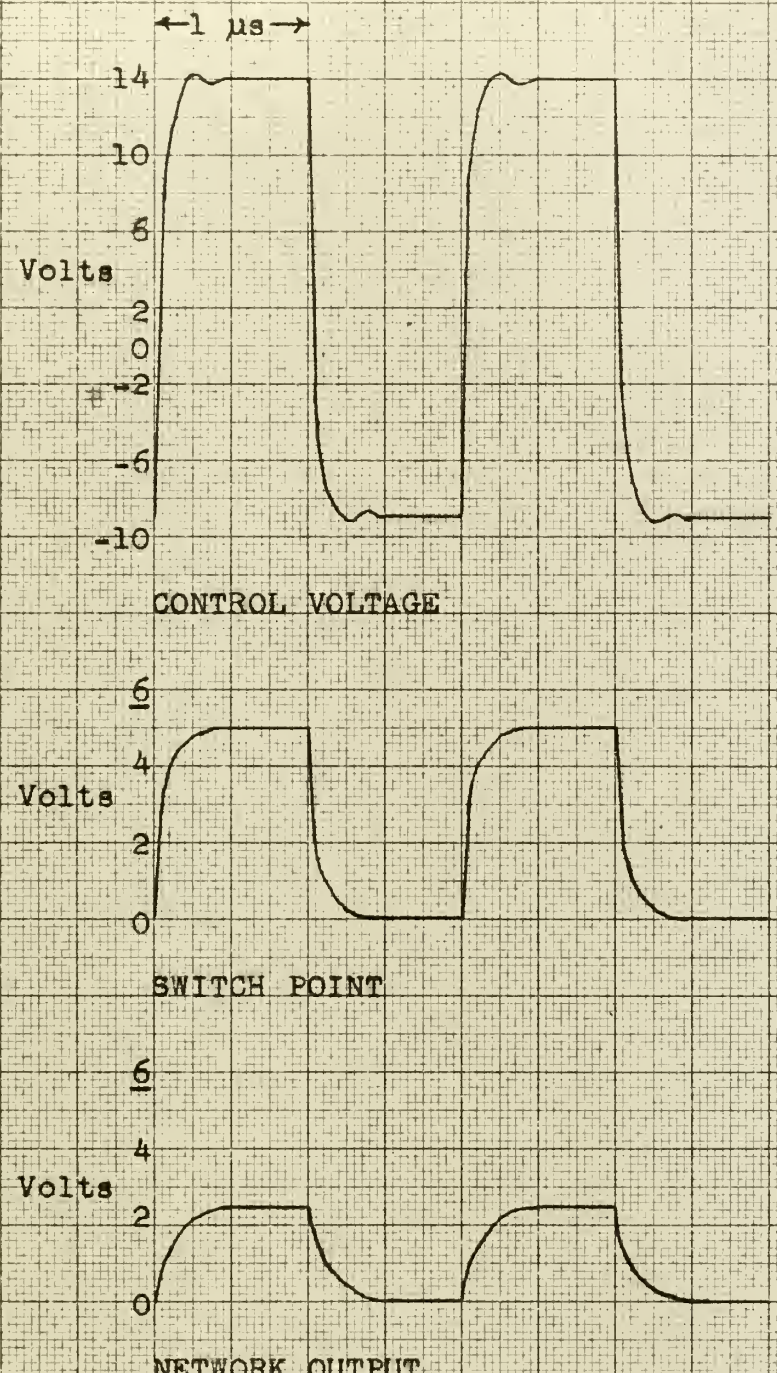
Diodes: 1N625

Ten-diode switch [4]

Figure 10

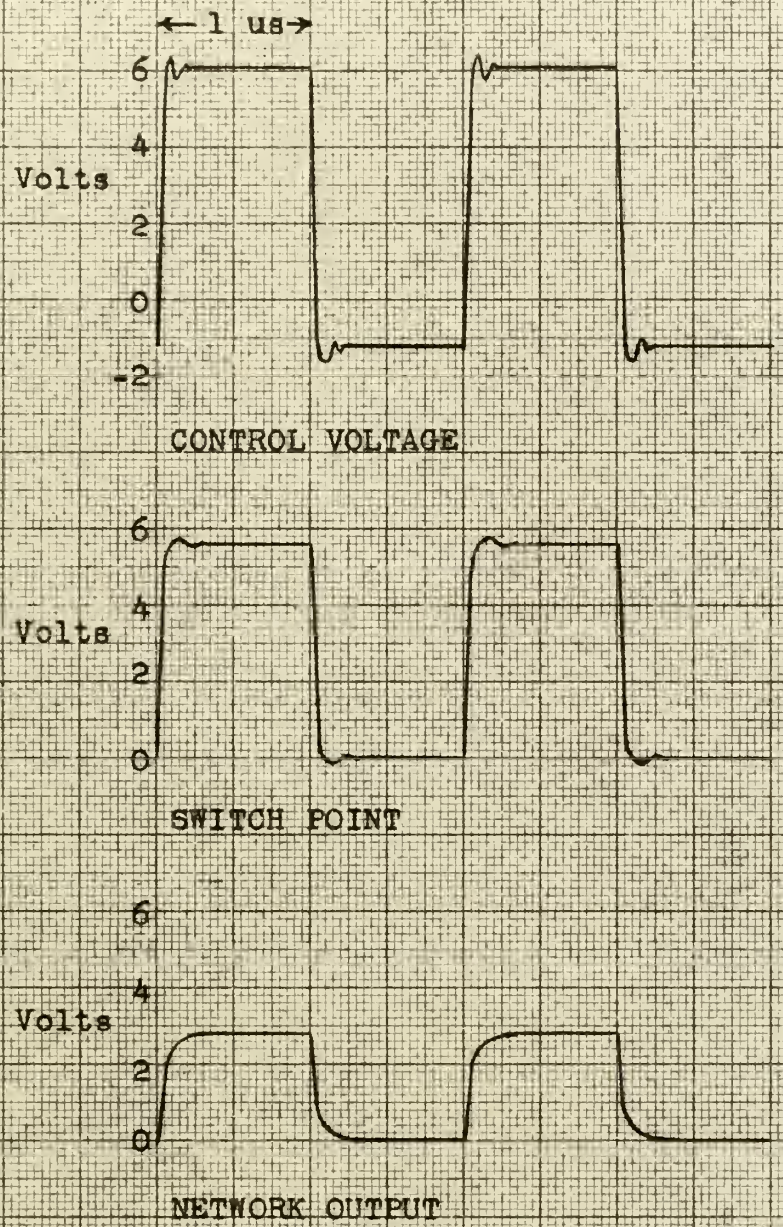
in order to raise the outputs from the register sufficiently to control the switch. The addition of ten active elements would increase power requirements and reduce system reliability. Figure 11 shows the waveforms in the switch and the weighting network for the four-diode circuit, using a square wave generator as the control source.

The other successful switch (Fig. 10) employs eight diodes in the two transmission gates and two diodes in the control input paths to the gates. This switch was designed originally by two British engineers [4] for use in an experimental system employing a current summing network. The disadvantages in the four-diode circuit are not found in this unit. The waveforms in Figure 12 show an improved speed of response and prove that it will perform its function with the toggle directly coupled to the control point of the switch. In the test circuit, no matching of the 1N625 diodes was attempted, and the switch was found to be stable under conditions of minor variations of the toggle output. In the single unit tested, errors in the switch were less than .2%. Each switch requires a maximum of 61.5 milliwatts of power.



Waveforms from four-diode switch

Figure 11

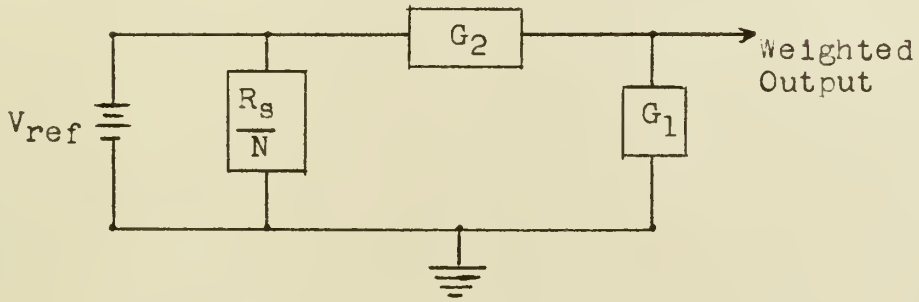


Waveforms from ten-diode Switch

Figure 12

6. COMPARISON OF CURRENT SUMMING AND VOLTAGE WEIGHTING TECHNIQUES

In Section 4, the basic concepts of the weighting network were discussed in terms of a current summing and a voltage technique. For purposes of comparison, the current summing network which was shown in Figure 6 will be used, as the resistance values for its weighting elements are chosen in the same manner as those for the voltage network. In the two examples, the equivalent circuit for the weighting net and switches combined is identical (Fig. 13).



Weighting network equivalent circuit.

Figure 13

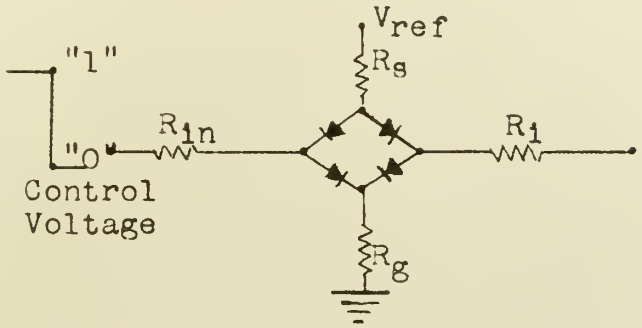
The nature of the switch employed in the unit is not relevant, since it will be the same switch for either method, normally. R_s/N is the parallel combination of resistors seen by the reference voltage at all times, where R_s is the resistance so labelled in Figures 9 and 10 and N is the number of bits in the system. G_2 and G_1 are the two combinations of weighting elements described in the voltage divider of Figure 7. The value of R_s must be chosen such that R_s/N is much less than the smallest value of resistance expected in the G_2 branch of the equivalent circuit. This requirement is necessary in order that V_{ref} will "see" an essentially

constant impedance under all conditions, thus making it a "virtual" constant voltage source. In this system, R_s/N is equal to 150 ohms.

If the voltage comparator presents a low input impedance to the output of the weighting network, the network acts as a current summing system. It can be seen that if the input impedance to the succeeding stage is sufficiently low, compared to the impedance of the G_1 path, the latter path may be eliminated from the equivalent circuit. The path through G_2 becomes a network of ten possible parallel branches which "divide" the total current into ten binary weighted increments of current. If, on the other hand, the input to the succeeding stage is high impedance compared to that of the G_1 path, essentially all the current through the G_2 path is also flowing through the G_1 path. In this instance, the system acts as a voltage divider. The voltage comparator can be designed to present either a high or low input impedance to the stage preceding it, so it is expedient to consider all the aspects of each system prior to selecting one in favor of the other.

The four-diode gate shown in Figure 14 can be used with a current weighting network but not with a voltage network. As pictured, a resistance is added to the value of the weighting resistor in the case when the switch point is in "ground" position. Such an addition is permissible in the current system, since the weighting resistor so switched is no longer in the circuit, to all intents and purposes. In

the voltage system, the weighting resistor is always a part of the circuit, and any additional resistance will produce unacceptable inaccuracies. In order to ensure a precise current, very careful selection processes and/or the use of trimmers will be a necessity.



Four-diode gate for current system [9].

Figure 14

The number of components required and the reliability of either weighting technique are similar. Input and output impedances of the network are identical. From Figure 13 it is obvious that the output admittance is always equal to the sum of the g's, or $1023(g_0)$ in the ten-bit system. The input impedance presented to V_{ref} is essentially constant and equal to R_s/N. Inaccuracies due directly to the switch or voltage supply are the same in either weighting method.

It may be well at this time to discuss the difference between "resolution" and "accuracy". Most contemporary articles concerned with ADCONs use the two words as synonyms. Resolution is a function of the number of bits in the system: for example, in a ten-bit system, the full scale to be measured may be divided into 1024 discrete portions (.1%). Theoretically, resolution may be improved indefinitely by

simply adding more bits. To imply .1% accuracy in a ten-bit system is tantamount to ensuring that all errors due to V_{ref}, switches, and weighting elements are considerably below .1% under the worst possible conditions. As the discussion progresses, it will become apparent that a practical limit of accuracy is reached at about .1%. It is considered that claims of 14-bit "accuracy" (.006%) may be described as a "gilding of the lily" and impractical in the present state of the art.

The main basis for comparison between the two methods is the consideration of errors to be expected in the weighting network as a result of errors in the weighting resistors only. Appendix B contains the supporting calculations for this comparison.

The current from the network at any instant is equal to $V_{ref} \times G_2$ (Fig. 13). In this comparison, the precision of the resistors will be chosen to be compatible with that presently obtainable, and considerations will be made on the assumption of random selection of components from a given lot. On this basis, errors will be assumed to be those expected when all components are at the limits of their respective precision. In the current technique, the errors in each element are additive, as the process itself is a summing operation. Assuming that all of the resistors were .1% precise, the total error of the system increases linearly, until it reaches .1% when the register is filled. Thus, a designer could not insure .1% accuracy without using a selection

program in the production process. For inputs of values near full scale, the .1% resolution offered by the use of ten bits would have been exhausted in .1% component error alone. The current error term is:

$V_{ref}(E_2)$.

The error term in the voltage technique is:

$Vref\left[E_2(1-G_2/G_t) - E_1(G_2/G_t)\right]$. (see Appendix B)

where E_2 and E_1 are the total errors in G_2 and G_1, respectively, and $G_t = G_1+G_2$. Whereas the current errors increase as the register fills, the error term for the voltage case is such that the coefficients of E_1 and E_2 change inversely as their multipliers. This fact means that the steady rise experienced by the current errors is compensated to a degree in the voltage method. Figures 15-19, at the end of this section, show plots of the maximum errors to be expected in each technique. From the curves, it can be seen that the voltage errors are considerably less than the current errors over a large portion of the operating range.

Case I is the "ideal" case, wherein all the resistors used are of .1% precision. Such an example may not be practical due to the expense and the difficulty of procuring .1% resistors whose values exceed 2M. Fortunately, the highest valued components in the network require the least precision. Case II embodies a relaxation of the precision requirements for several of the large value elements. These changes are tabulated in the appendix. Figure 16 shows that the voltage errors are much less than those for the current

network in this case. Actually, the current errors exceed .1% over a considerable part of the full range.

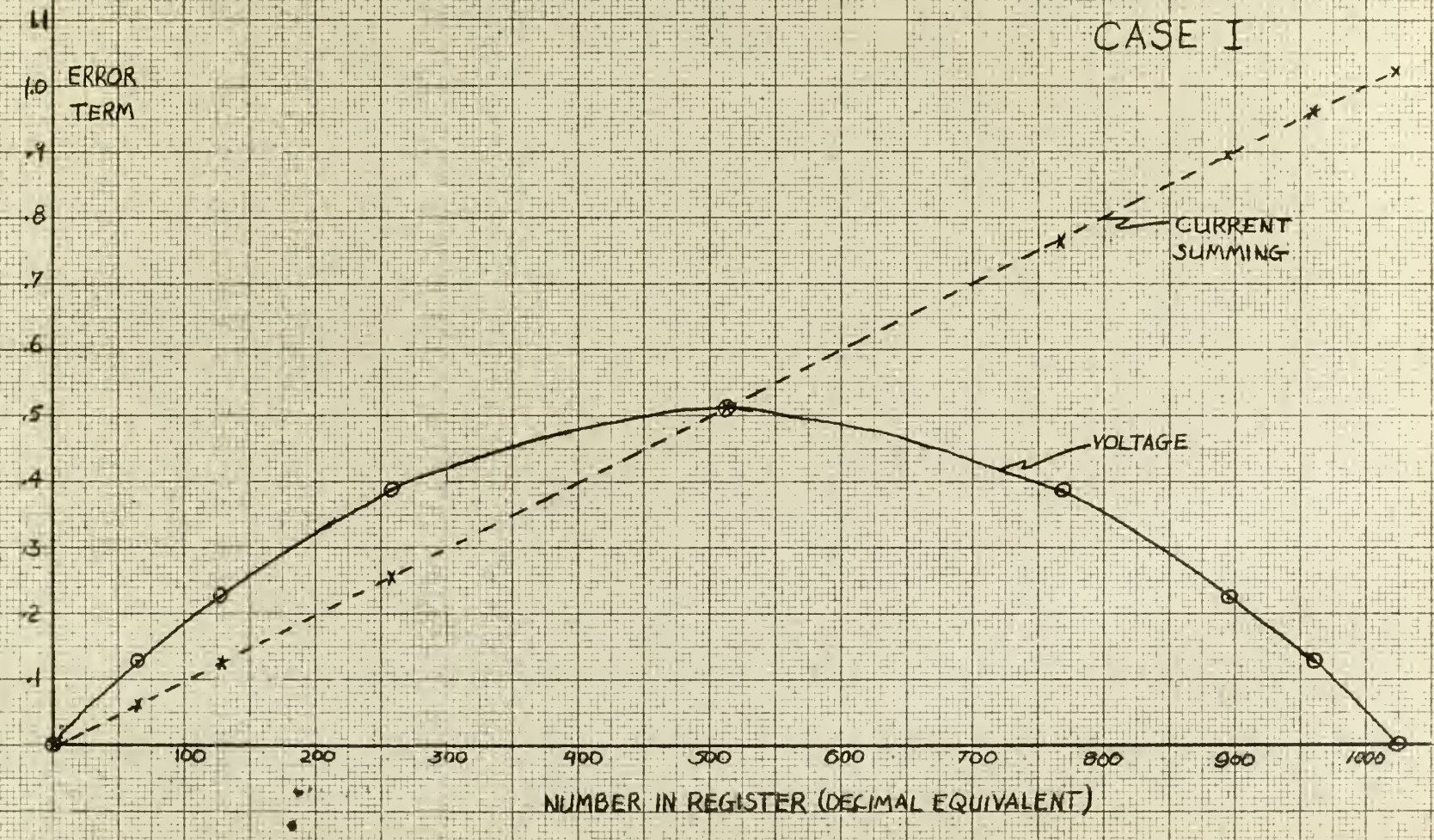
Normally, even random selection of components would not produce the situation of these maximum errors, but a manufacturer cannot claim a greater accuracy unless selection is used to ensure the requisite maximum error to be expected. Regardless of the complexities chosen for the production of the unit, the results show that under identical circumstances greater accuracy can be achieved with the voltage technique.

This system has been designed for low level inputs, and it has been found that accurate voltage increments can be produced at low levels. Using a V_{ref} of five volts, as in the designed system, the current network would produce a least increment of current of about one microampere. In a ten-bit system, the values for the weighting resistors cannot be reduced below those selected for this system without jeopardizing the maintenance of the "constant" voltage source for V_{ref}. Larger currents could be realized by increasing V_{ref}, but such a course of action would increase the power requirements of the system and eliminate the existing capability of direct coupling the toggles to the switches. The weighting network and switches designed herein require a maximum of .78 watts of power; the DACON will require about four watts maximum. Thus, it is considered that the voltage weighting technique is superior in terms of accuracy and in applications specifying low power and low level inputs.

FIGURE 15

ERROR TERM VS
NUMBER IN REGISTER

CASE I



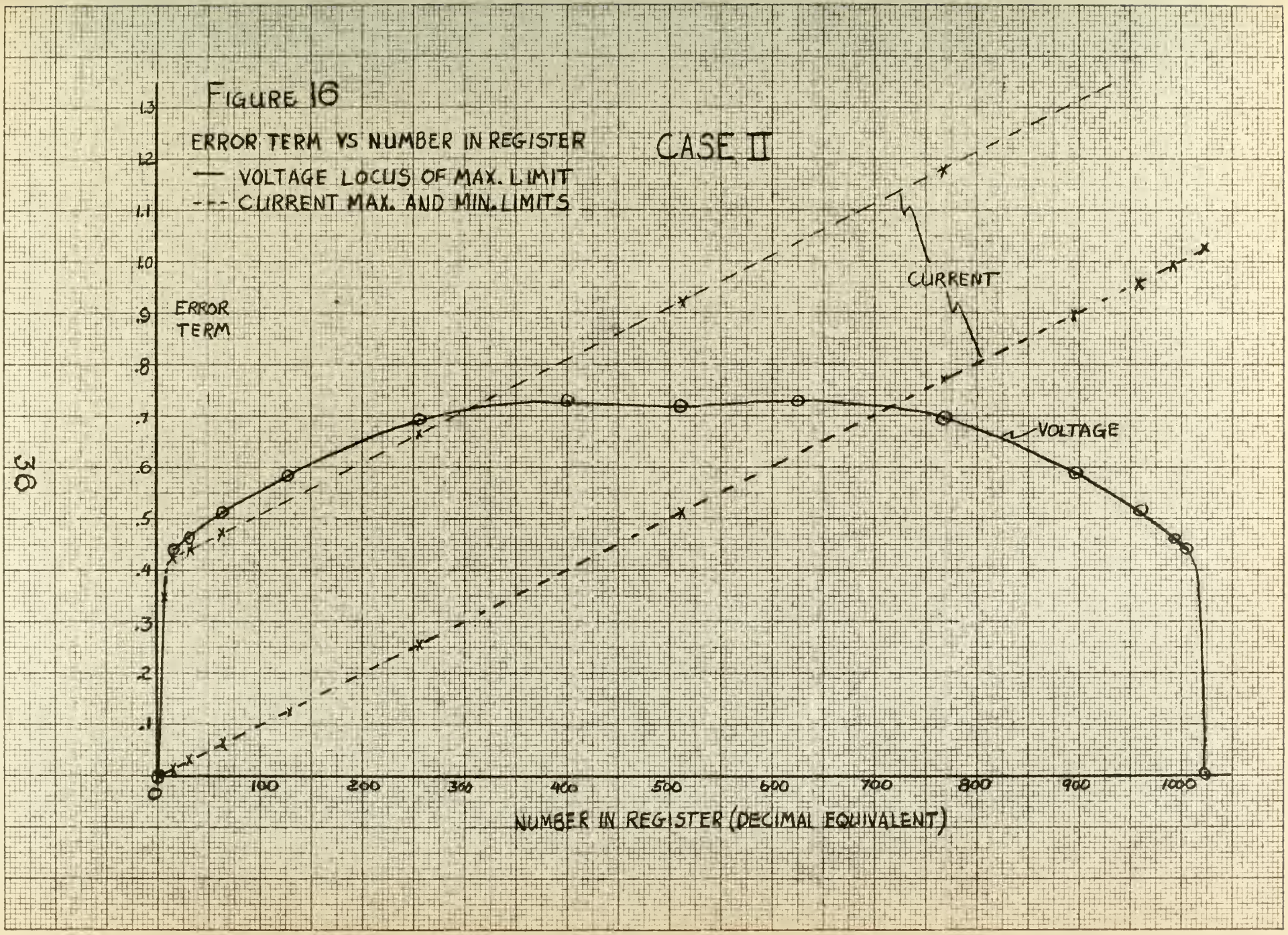


FIGURE 16
ERROR TERM VS NUMBER IN REGISTER
CASE II
— VOLTAGE LOCUS OF MAX. LIMIT
--- CURRENT MAX. AND MIN. LIMITS
ERROR TERM
CURRENT
VOLTAGE
1.3
1.2
1.1
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
100
200
300
400
500
600
700
800
900
1000
NUMBER IN REGISTER (DECIMAL EQUIVALENT)

FIGURE 17

DETAILS OF SECTION FROM FIGURE 10

—o— VOLTAGE

---x--- CURRENT

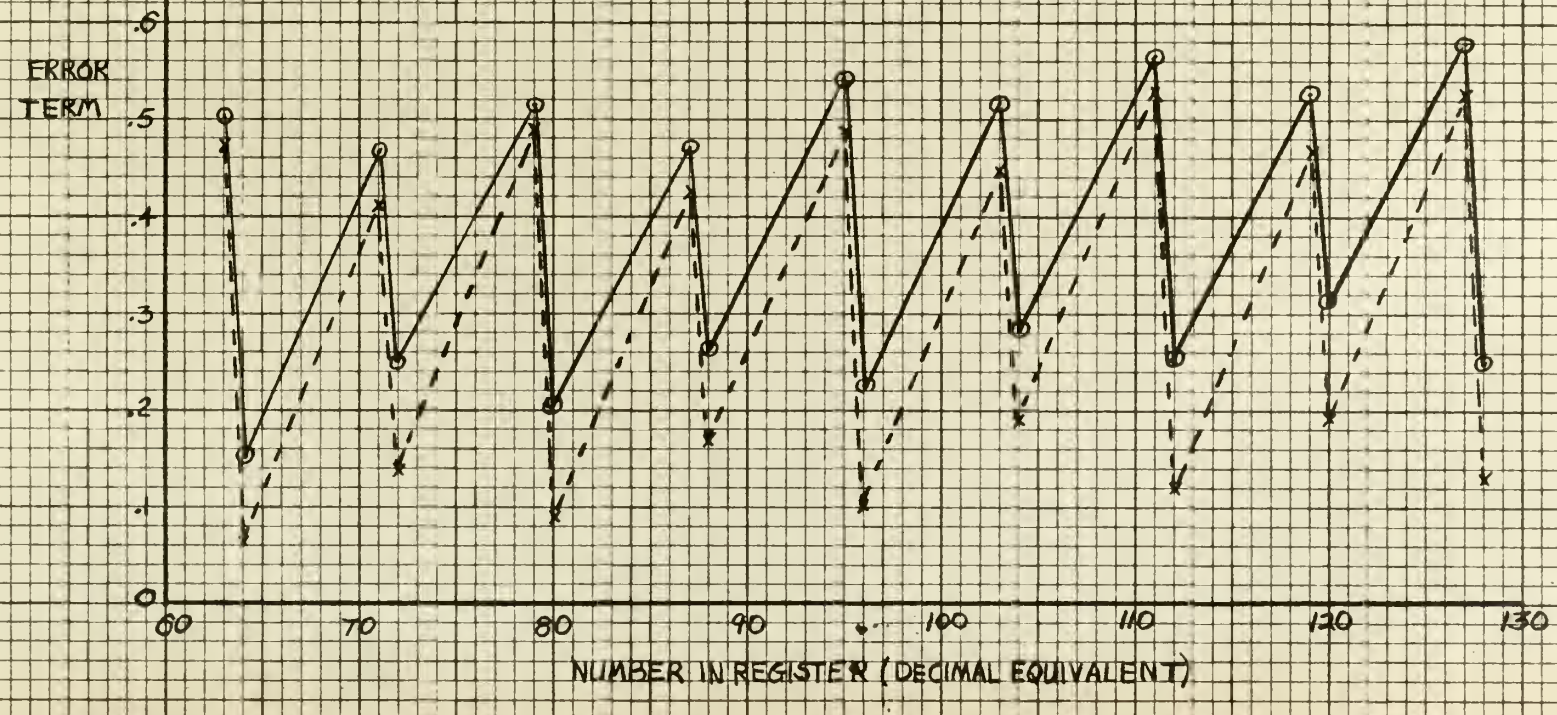
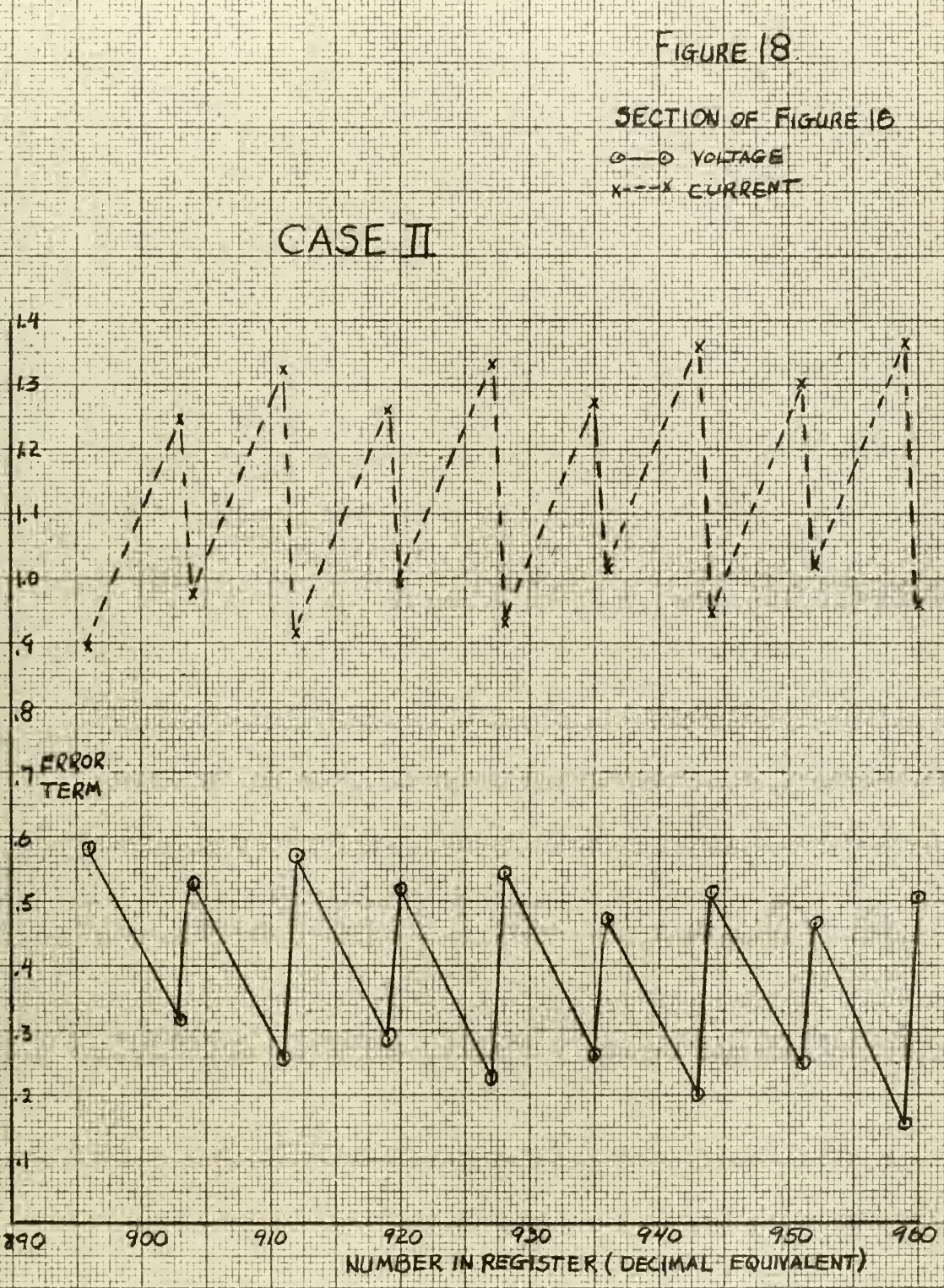
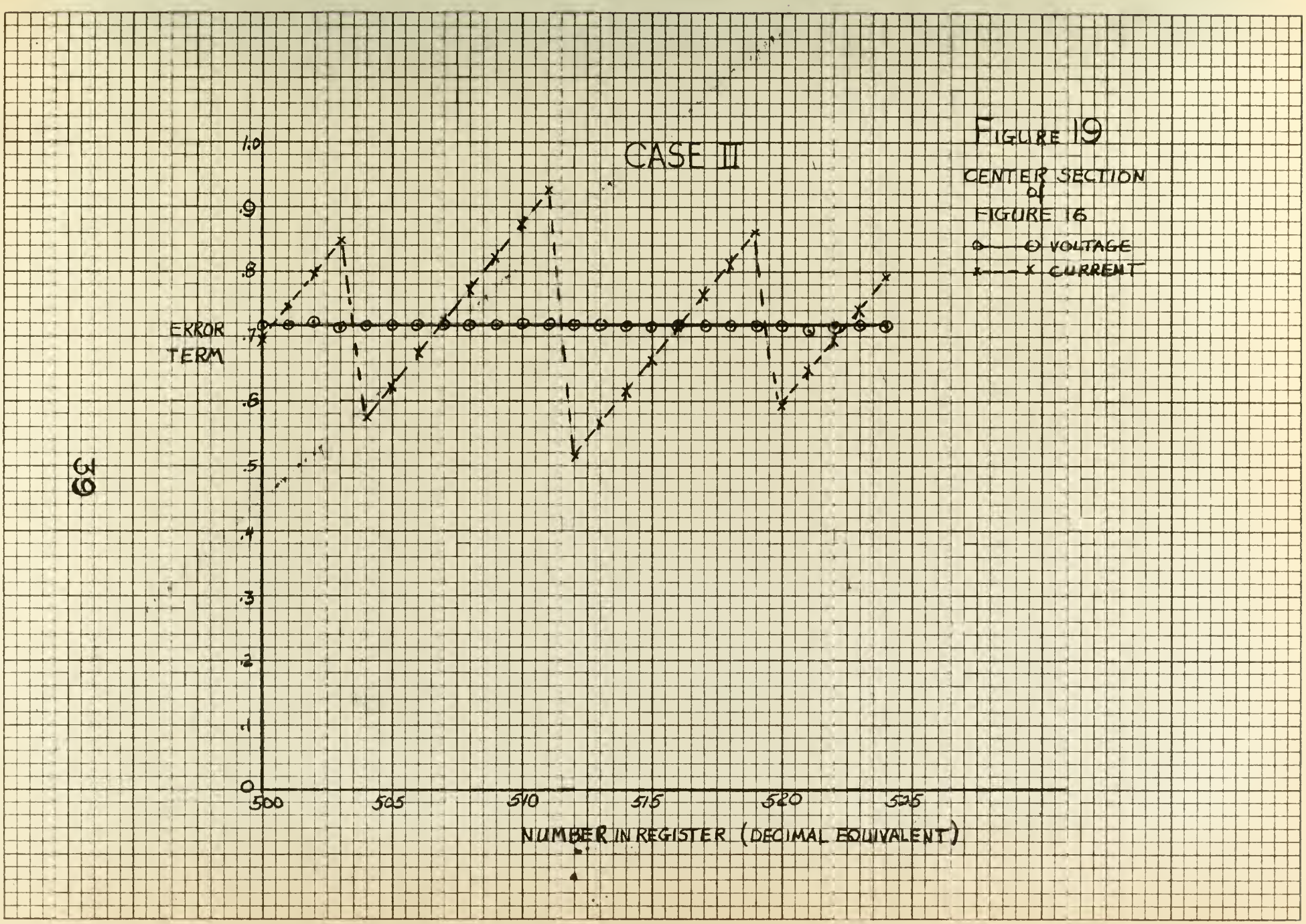


FIGURE 18.


SECTION OF FIGURE 18
VOLTAGE
CURRENT
CASE II
1.4
1.3
1.2
1.1
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
ERROR TERM
890
900
910
920
930
940
950
960
NUMBER IN REGISTER (DECIMAL EQUIVALENT)


CASE II
FIGURE 19
CENTER SECTION
OF
FIGURE 16
VOLTAGE
CURRENT
ERROR
TERM
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
500
505
510
515
520
525
NUMBER IN REGISTER (DECIMAL EQUIVALENT)

7. VOLTAGE COMPARATOR AND LOGIC NETWORK

Earlier, it was stated that a voltage comparator existed which possessed the sensitivity required of the specified converter. Figure 20 contains the schematic of an error amplifier incorporated in a converter designed by Radiation Incorporated [9]. It is a transistorized difference amplifier whose stated sensitivity of plus or minus five millivolts is precisely that required of a ten-bit, five volt system. This circuit can be redesigned to present a high input impedance to the weighting network, yet retain its sensitivity and stability.

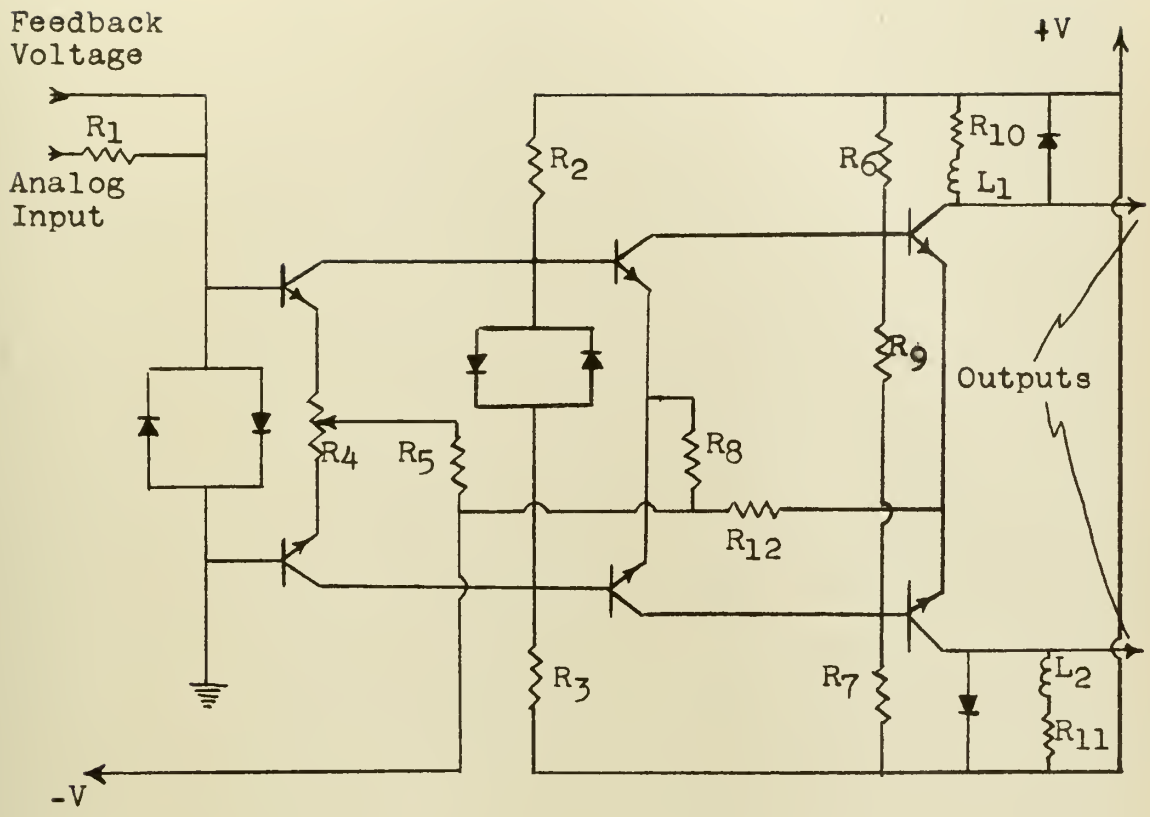
The logic network is straightforward, consisting of a one megacycle clock, a ring counter, and ten AND gates. The steps required of the logic are as follows:

Step 1: Set T_9; reset T_8-T_0. (D_1=A_9, B_8,B_7,- - B_0)

Step 2: If V_{in} less than V_{fdbk}, reset T_9. ($Z \cdot D_2$=B_9)
Set T_8. (D_2=A_8)

Steps 3-10: same as Step 2, treating successive toggles in order.

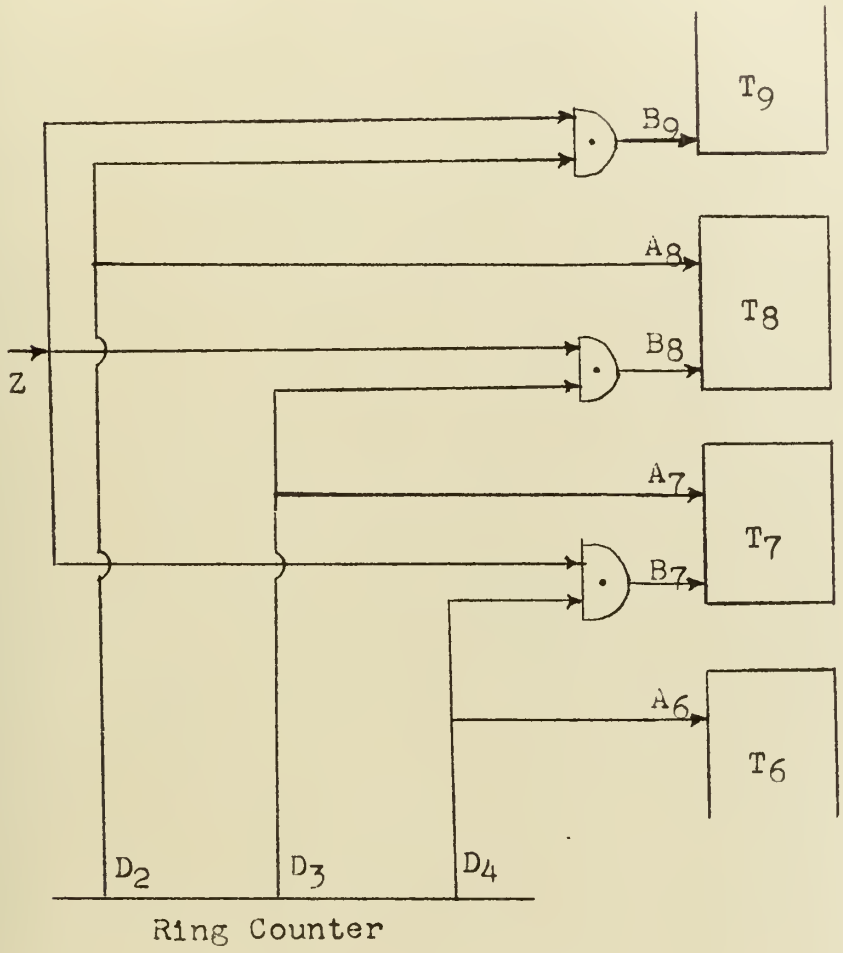
Figure 21 shows a portion of the logic circuitry, which will be duplicated for each toggle. The logic required for "readout" has not been included, as this will vary in accordance with the demands of the system in which the converter may be used. In order to accomplish "readout" an additional digit time will be required; for serial "readout" all but the least significant bit will have been read out in ten digit times through the use of time sharing, and for parallel



Error amplifier (Radiation, Inc.) [9]

Figure 20

"readout" the entire register may be read out in a single additional digit time. The time shared serial "readout" may be accomplished as follows: T_9 during D_2, T_8 during D_3, and so on until T_0 during the added D_{11}.



Sample logic circuitry for T_8 and T_7.

Figure 21

8. CONCLUSIONS

An analog-to-digital converter which meets the specifications established at the outset of this investigation is feasible at this time. Due to its inherent low power demands and to the use of a minimum number of active components, it is capable of being packaged in a size compatible with telemetering applications in airborne vehicles. Its accuracy approaches the precision suggested by the 1/1024 resolution of the ten-bit system. Although its speed of conversion is not at the limit of capability for a feedback encoder, it approaches that limit while using "on the shelf" components.

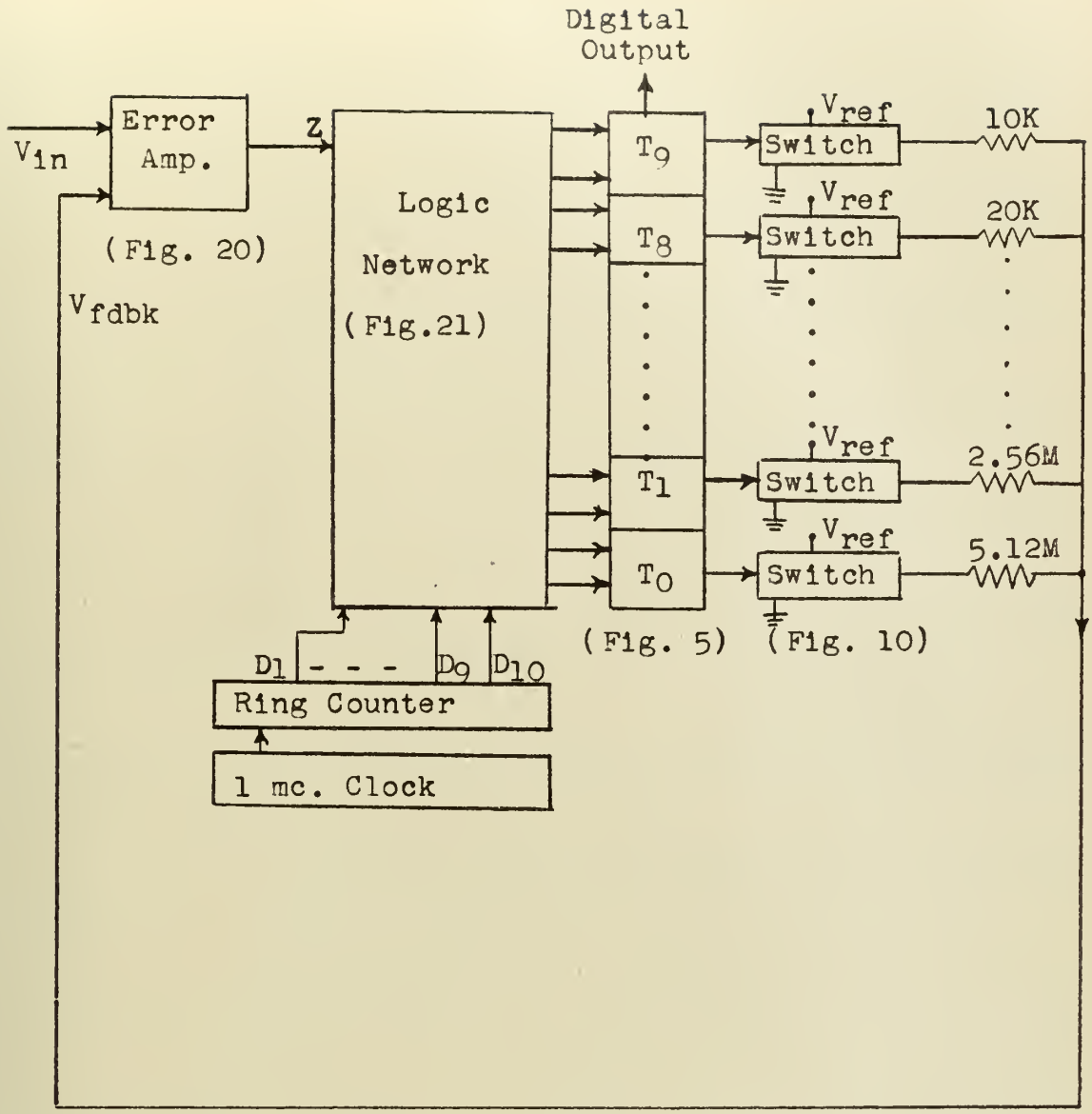
The use of the voltage weighting network ensures higher degrees of accuracy than those which can be expected of a current summing network under similar circumstances of production and design. The voltage technique lends itself to greater ease of design for systems in which low level inputs are expected. However, even with the improvement in accuracy afforded by a voltage weighting network, it is considered that this system represents the practical limit of accuracy which can be expected from feedback encoders at this time. For example, a 14-bit system offers .006% resolution, but in order to achieve this degree of accuracy, the designer must incorporate a reference voltage supply whose regulation is better than six parts in one hundred thousand, assuming no errors in the switches or the weighting resistors. From the results shown in the curves of Section 6 and on the basis of a realistic production process, attempts to

achieve greater system accuracies than .1% are impractical with the components presently available.

Discussion of the converter has not included the sampling problem at the input, the voltage supply problem, nor the environmental stability problem. The assumption is that these problems have been solved independently or will be solved in the near future. The high conversion speed of this system will necessitate the incorporation of an electronic commutator; a design problem which is being widely investigated at the present time.

It is recommended that the components described herein be assembled and tested as a system, and that the sampling problem as it applies to this system be studied further. The realization of an ADCON such as this unit can mean the ultimate achievement of "real time" telemetering systems and correlators in the immediate future.

Figure 22 shows a more detailed block diagram of the feedback converter, after filling the blocks originally outlined in the functional picture of Figure 4.



Block diagram of ten-bit, 100 kc. ADCON

Figure 22

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APPENDIX A

MULTIVIBRATOR DESIGN STEPS

The reasons for selecting the 2N247 Drift Transistor have been given in Section 3. The initial choice for V_{cc} was -24 volts in order to allow a safety margin with respect to the maximum of -35 volts specified by RCA. V_{bb} is chosen to be at ground potential in order to reduce the number of power supplies needed in tests of the circuit. All initial calculations are made as if the transistor were NPN in order to simplify the calculations of branch currents at nodes in the circuit. When using a PNP transistor, as in this circuit, all values of voltage supply are simply changed in sign.

Due to the excessive storage time of the 2N247, the circuit is designed as a non-saturating multivibrator. The collector-base potential must not go below six volts. It is desirable to keep the value of R_L as low as possible in order to optimize the rise time of the output pulse. A current of five milliamperes will provide a large swing with the low value of R_L. The design philosophy is to use a common emitter resistor for both switching transistors to keep the potential at both emitters constant for both states of the circuit. The emitter followers are inserted for the reasons given in Section 3. R_L is chosen to be 1.5K initially. The collector of the "off" transistor will be about 23 volts.

I_c = Collector current. V_C = collector-ground potential

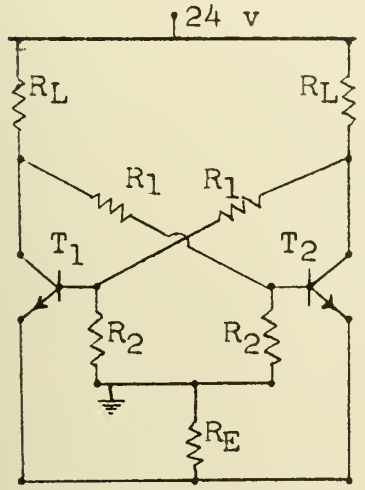
I_b = Base current V_B = base-ground potential

I_e = Emitter current V_E = emitter-ground potential

$I_c \times R_L$ = voltage drop across R_L of "on" transistor.

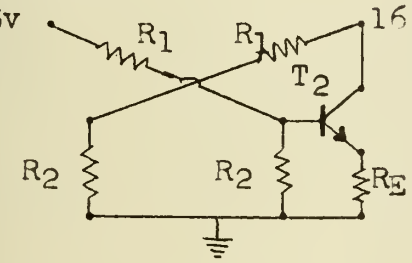
$5 \times 10^{-3} \times 1.5 \times 10^3 = 7.5$ volts

$V_{Con} = V_{cc} - (I_c \times R_L) = 24 - 7.5 = \underline{16.5}$ volts.



The circuit may be considered without the emitter followers, as shown, because $V_E \cong V_B = V_C$ of the switching transistor.

$\underline{T_1}$ "off":



Current equal to 3 ma. is chosen for R_1+R_2 path from "off" collector.

$R_1+R_2 = 23/3 \times 10^{-3} = \underline{7.67K}$

I_{b2} is negligible.

Let V_{B2} = 3 volts. $(R_2/R_1+R_2)23$ v = 3 v. $R_2 = 3 \times 7.67K/23 = \underline{1K}$

$R_1 = 7.67K - 1K = \underline{6.67K}$

Select RMA values of 6.8K and 1K for R_1 and R_2, respectively.

$V_B = 23(1/7.8) \cong \underline{2.95}$ volts. $V_E \cong \alpha V_B \cong .95 \times 2.95 = \underline{2.7}$ volts

$I_e \cong I_c = 5$ ma. $R_E = V_E/I_e = \underline{540}$ ohms. Use 560 Ω RMA.

Due to the fact that R_E is a common resistor to both

emitters and that V_E will remain constant, essentially, I_e will be maintained at 5 ma. and will keep I_c constant at about the same value. Check to see if T_1 is cut off:

$V_{B1} = (1/7.8)16.5 = 2.11$ volts

$V_{B-E} = 2.11-2.7 = -.59$ volts. T_1 is cut off.

The characteristics of the 2N247 allow a maximum of -1 volt dc base-emitter voltage; thus, the diodes were inserted from base to emitter of each switching transistor as a safety measure to protect the junction.

The maximum collector dissipation in this circuit was 65 milliwatts which exceeded the maximum rating of the 2N247; R_L and R_E were increased by the same proportion to 3.3K and 1.3K, respectively, in order to reduce I_c and maintain all voltages throughout the circuit at their original values. The output remained essentially the same, and the dissipation was reduced to a satisfactory value. Maximum collector dissipation for the 2N247 is:

80 mw	25° C
50 mw	50° C
35 mw	70° C

The value of the collector voltage supply was increased to -31 volts in order to achieve the final output swing of about nine volts. V_{cc}, V_{bb}, and V_{ef} were changed by the same amount to those given in Figure 5 in order to shift the output in such a way as to have one level on either side of dc ground to produce the necessary control voltages for the switch.

APPENDIX B

ACCURACY COMPARISON

Figures 15-19 are the graphical results of the errors which are tabulated in this appendix. Two cases have been used in the comparison:

Case I; all weighting resistors are of .1% precision.

Case II; the same as Case I except for the following:

r_3, 1%; r_2-r_0, 5% precision.

The error terms associated with each technique were determined as follows:

CURRENT	VOLTAGE
$I = G_2 x Vref$	$v = (G_2/G_t)Vref$
$I = Vref(G_2+E_2)$	$v = Vref\left[(G_2/G_t) + \frac{E_2(1-\frac{G_2}{G_t})-E_1(\frac{G_2}{G_t})}{G_t+E_1+E_2}\right]$
Error term = $\underline{E_2}$.	Error term = $\underline{E_2(1-G_2/G_t)-E_1(G_2/G_t)}$.

Note:

e_i: error in g_i or r_i=precision x g_i or r_i; i=0,1,....9.

E_1: sum of e's for elements which constitute G_1.

E_2: sum of e's for elements which constitute G_2.

G_t: G_1+G_2.

Maximum error for current technique occurs when all e's are at limit of precision and are of the same sign.

Maximum error for the voltage technique occurs when all e's are at the limit of precision and E_1 differs in sign from E_2 to make the numerator of the error term a maximum.

COMPONENT VALUES AND MAXIMUM e's.

g_i	Rel. Value	Precision(%) Case I	Precision(%) Case II	Inc. Error(e_1) Case I	Inc. Error(e_1) Case II	Actual Value (Ω)
g_9	512	.1	.1	.512	.512	10K
g_8	256	.1	.1	.256	.256	20K
g_7	128	.1	.1	.128	.128	40K
g_6	64	.1	.1	.064	.064	80K
g_5	32	.1	.1	.032	.032	160K
g_4	16	.1	.1	.016	.016	320K
g_3	8	.1	1.0	.008	.080	640K
g_2	4	.1	5.0	.004	.200	1.28M
g_1	2	.1	5.0	.002	.100	2.56M
g_0	1	.1	5.0	.001	.050	5.12M

SAMPLE CALCULATION: Case II

Binary Number	Decimal Equiv.	$\frac{G_2}{G_t}$	E_2	Voltage Error Term $E_2(1-G_2/G_t)+E_1(G_2/G_t)$
0111110100	500	.489	.696	.696(.511)+.742(.489)=.717
0111110101	501	.490	.746	.746(.510)+.692(.490)=.720
0111110110	502	.491	.796	.796(.509)+.642(.491)=.721
0111110111	503	.492	.846	.846(.508)+.592(.492)=.710
0111111000	504	.493	.576	.576(.507)+.862(.493)=.717
0111111001	505	.494	.626	.626(.506)+.812(.494)=.717
0111111010	506	.495	.676	.676(.505)+.762(.495)=.719
0111111011	507	.496	.726	.726(.504)+.712(.496)=.720
0111111100	508	.497	.776	.776(.503)+.662(.497)=.719
0111111101	509	.498	.826	.826(.502)+.612(.498)=.720
0111111110	510	.499	.876	.876(.501)+.562(.499)=.720
0111111111	511	.500	.926	.926(.500)+.512(.500)=.719

LOCI OF MAXIMUM ERROR TERMS

Decimal Equiv.	Error Term			
	Current		Voltage	
	Case I	Case II	Case I	Case II
1	.001	.050	.002	.051
3	.003	.150	.006	.154
7	.007	.350	.014	.353
15	.015	.430	.030	.435
31	.031	.446	.062	.462
63	.063	.478	.126	.508
127	.127	.542	.224	.586
255	.255	.670	.384	.696
511	.511	.926	.511	.719
767	.767	1.182	.384	.696
895	.895	1.310	.224	.586
959	.959	1.374	.126	.508
991	.991	1.406	.062	.462
1007	1.007	1.422	.030	.435
1015	1.015	1.358	.014	.353
1019	1.019	1.238	.006	.154
1021	1.021	1.338	.002	.051